REMARKS

Reconsideration of the application is respectfully requested.

Claims 1-22 stand rejected as being either anticipated or obvious in view of U. S. Patent 4,709,259 to Suzuki ("Suzuki '259") and U. S. Patent No. 6,175,383 to Yadid-Pecht ("Yadid-Pecht '383"). In this amendment, claims 1-22 are cancelled and replaced by new claims 23-30. It is noted that these new claims present no new matter, as they are supported by the specification as filed, at page 7 line 1 to page 8 line 21.

New claim 23 is directed to an integrated circuit that includes a color sensor array, a reset shift register, and a wordline shift register. The reset shift register is coupled to control a reset of sensor elements, and the wordline shift register is coupled to control a readout of the sensor elements. Control logic is coupled to feed the reset shift register with a pair of reset bits. In addition, the wordline shift register is to be fed with a read bit. The shift registers are operated so that the pair of reset bits and the read bit shift through their respective registers, while an image frame is being captured. One of the reset bits remains one or more rows behind the read bit, to generate a correlated double sampling pixel reset value after each pixel integrated intensity value is generated. The other reset bit is one or more rows ahead of the read bit, to mark the start of integration. Neither Suzuki '259 or Yadid-Pecht teaches or suggests such a circuit.

The color image sensor described in Suzuki '259 has blue, green, and red color vertical scan shift registers 130a – 130c to vertically scan each color. Suzuki '259, column 4 lines 27-68 . In operation, the red vertical scan shift register 130c outputs a

shift pulse from the first output terminal D1 to supply it to the red horizontal line 141c see Suzuki '259, Fig. 1. In this state, the red horizontal scan shift register 131c scanned once to sequentially turn on the red MOS switches 161c to 166c. The charge signals stored in the red photodiodes 11 and 14 in the first row are sequentially read as analog signal, which in turn are sent via the red output line 170c to an A/D converter (not shown). Suzuki '259, column 5 lines 41-56.

After completion of the readout of the red photodiodes in the first row, the red vertical scan shift register 130c outputs a shift pulse from the second output terminal D2. In this state, the red horizontal scan shift register 131c scans once as described above, to read the charge signals stored in the photodiodes in the second row. Similarly, the red photodiodes in the third and following rows are scanned to sequentially read the red charge signals.

However, Suzuki '259 does not teach or suggest Applicants' claimed integrated circuit in new claim 23, in which a reset shift register and a wordline shift register are used in such a way that a pair of reset bits in the reset shift register and a read bit in the wordline shift register shift through their respective registers while an image frame is being captured, with one of the reset bits being behind the read bit, to generate a correlated double sampling pixel reset value after each pixel integrated intensity value, and the other reset bit being ahead of the read bit to mark the start of integration.

As to Yadid-Pecht, although this reference mentions that dynamic range of active pixel sensors may be widened via control over integration time, where integration time begins with a reset signal and ends with a sample signal, where both column reset and row reset signals are used for independently resetting any pixel address within the

array without interfering with the readout process, this does not teach or suggest the circuitry recited in Applicants' new claim 23.

Turning now to new claim 27, this claim is directed to a system having a color sensor array, a reset shift register, a wordline shift register, and control logic coupled to feed the registers with reset and read bits that operate as recited. There is no suggestion to modify the shift registers of Suzuki '259 to read on the circuitry in new claim 27 where pixel levels are read from the array one row at a time. In addition, Yadid-Pecht does not teach or suggest modifying the row and column control circuitry so as to meet the limitations of new claim 27.

The new dependent claims are submitted as not being anticipated or obvious, for at least the reasons given above in support of their base claims 23 and 27.

In sum, a good faith attempt has been made to present claims that are submitted to be in condition for allowance.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on April 22, 2003.

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